PHYSICS PRACTICAL SHEETS

VARIETY PRODUCT

Date: 2078/07/07 ... Prime ... CAMPUS
Class: B.Sc. CSIT
Roll No.:
Shift: Morning
Object of the Experiment (Block Letter)

Experiment No.: 5
Group:
Sub.:
Set:

TO STUDY RS FLIP-FLOP BY USING BREADBOARD.

APPARATUS REQUIRED:

i) BreadBoard
ii) Power supply
iii) Multimeter
iv) 7400 IC
v) LED (Light Emitting Diode)

THEORY:

The basic memory digital circuit is called flip-flop. It has two stable state, either high '1' or low '0'. It can be constructed by using NAND or NOR gate.

The flip-flop is said to be memory circuit since its Inputs will remain as set until some operation is done to it. As such flip-flop can be used to store one bit. For instances if the flip-flop is said to be low stable state, it can be regarded as storing a logic.

Four NAND gates are connected as shown in fig to form a RS flipflop circuit. The flip flop has usually two outputs Q and $\overline{Q}$. The inputs and outputs possibilities for RS flipflop are summarized in the truth table given below:

SN	R	S	Q	Comments
1	0	0	last state	No change
2	0	1	1	set
3	1	0	0	Reset
4	1	1	?	Forbidden

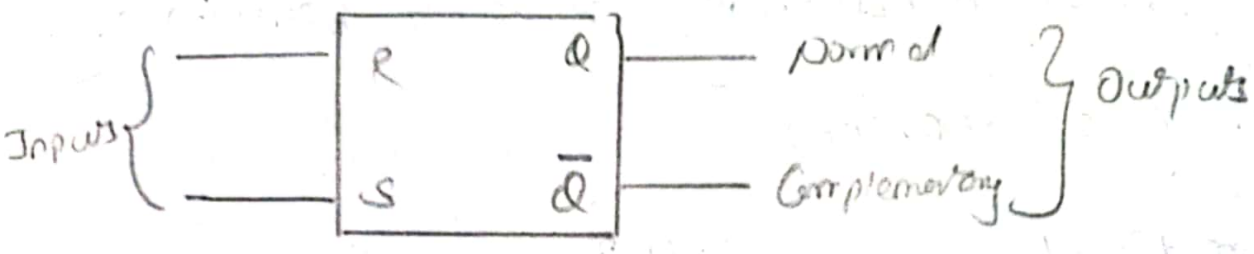

fig. logic diagram of RS flipflop

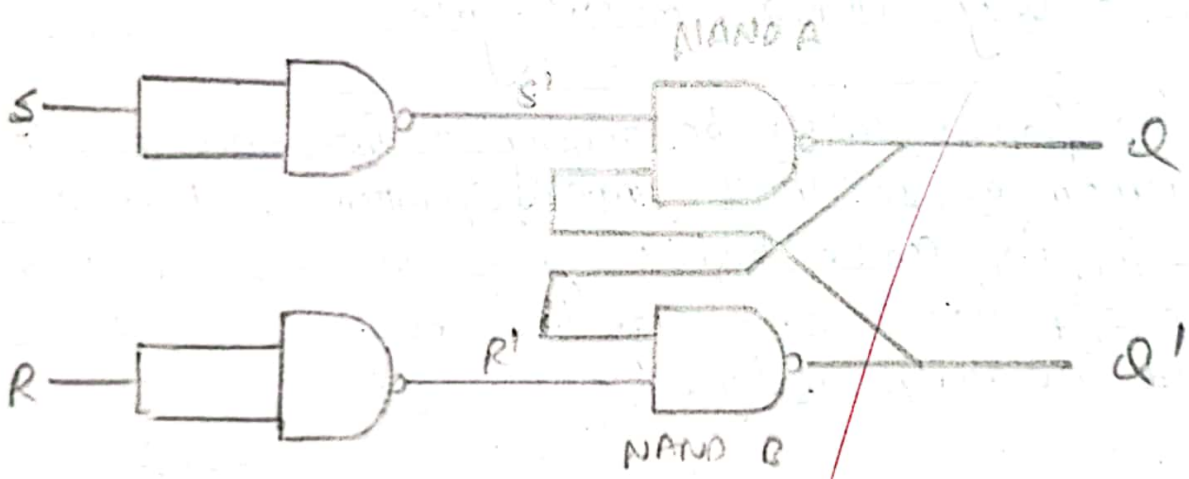

fig Circuit diagram of RS flipflop using NAND gates.

For R=0, S=0, NAND gate has no effect on its output. The flipflop simply remains in its last state. The second input conditions are R=0 and S=1, the output of NAND A is high and B is low. Thus, '1' at 'S' input is said to be set flipflop and it switches to the stable state where Q=1 and $\bar{Q}$=0. The third input condition is R=1 and S=0. This condition forces the output of NAND gates A low & B high. Thus 1 at R input is said to be reset. That is it switches state Q=0 and $\bar{Q}$=1. The last condition is R=1 and S=1 is forbidden. as it forces the output of both NAND gates to high, ie Q=1 & $\bar{Q}$=1. But it violates the basic definition of flipflop that requires the Q to be complement of $\bar{Q}$.

OBSERVATION:

R (±0.1V)	S (±0.1V)	Q (±0.1V)	$\bar{Q}$ (±0.1V)	Comment
0	1	0.2	3	set
1	0	3	0.2	reset
0	0	0.2	3	No change
1	1	0.2	0.2	forbidden

RESULT:

From the above observation table, we can see that the truth table for RS flipflop is satisfied with the observed value i.e in the table, the supply voltage is 5V and output high is 3V and output low is 0.2V which is slightly different from exact supply.

CONCLUSION:

Here, we supplied input voltage 5V on high (1) and on low (0). But the output isn't exactly 5V and 0V. For high & low different conditions, it is different from the expected values due to drop on the transistor and resistor used in the given IC. That means flipflop is also known as memory device and can be used to store one bit.

PRECAUTIONS:

i) The wires should be connected properly.
ii) The measurement must be taken accurately.
iii) The wires should not be loose.