PHYSICS PRACTICAL SHEETS

Date: 2078/07/07 Prime CAMPUS
Class: BSc. CSIT
Roll No.:
Shift: Morning
Object of the Experiment (Block Letter)

Experiment No.: 4
Group:
Sub.:
Set:

VARIETY PRODUCT

TO DESIGN AND STUDY THE LOGICAL GATES USING NOT, AND, OR, NOR & NAND BY TTL.

APPARATUS REQUIRED:

i) Diodes
ii) Transistors (BC 547C)
iii) Breadboard
iv) Jumper wires
v) Multimeter
vi) Power supply DC(5V)

THEORY:

Logic gates are the elementary building blocks of any digital system. These are electronic circuit having one or more than one input and only one output & responds only to HIGH voltage or LOW voltage. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as OR gate, AND gate, NOR gate & NAND gate. First three are basic gates, whereas last two are universal gates.

1) AND Gate:

The AND gate is sometimes called the "all or nothing gate". When all inputs are HIGH, then output is HIGH, else output is LOW.

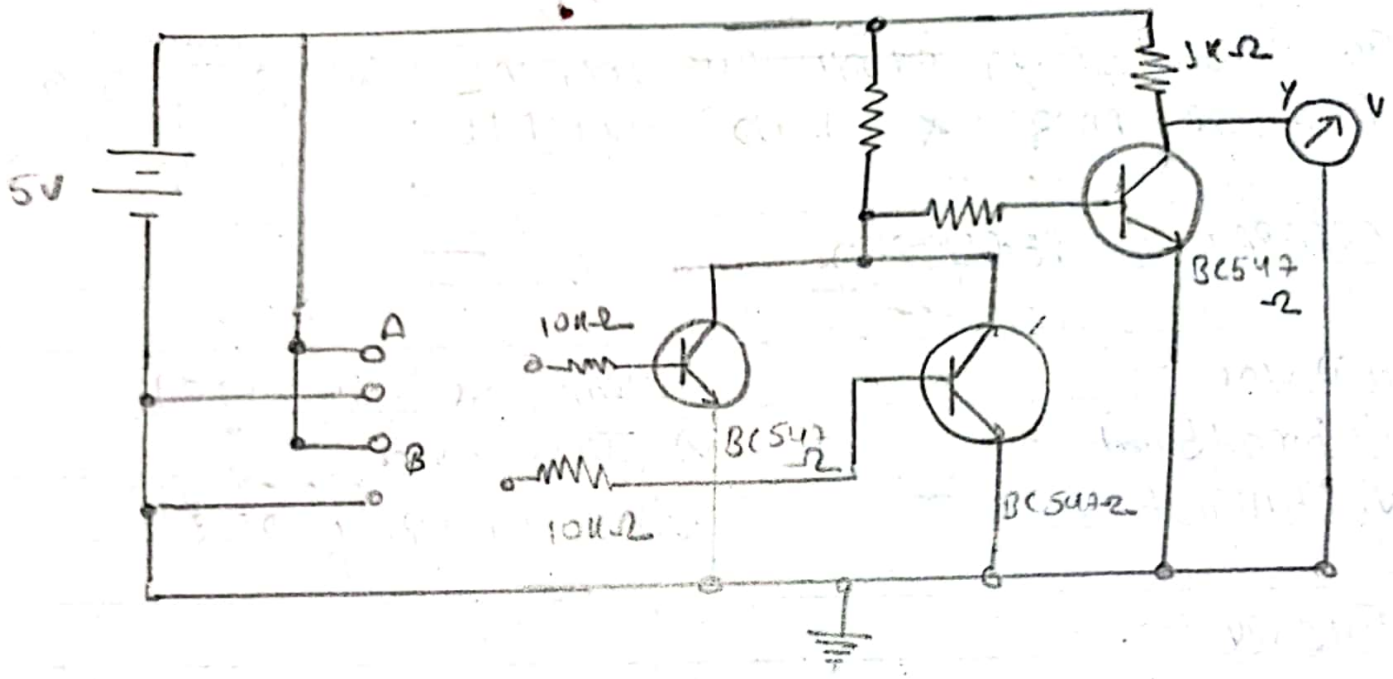


fig. Experimental circuit diagram for OR Gate

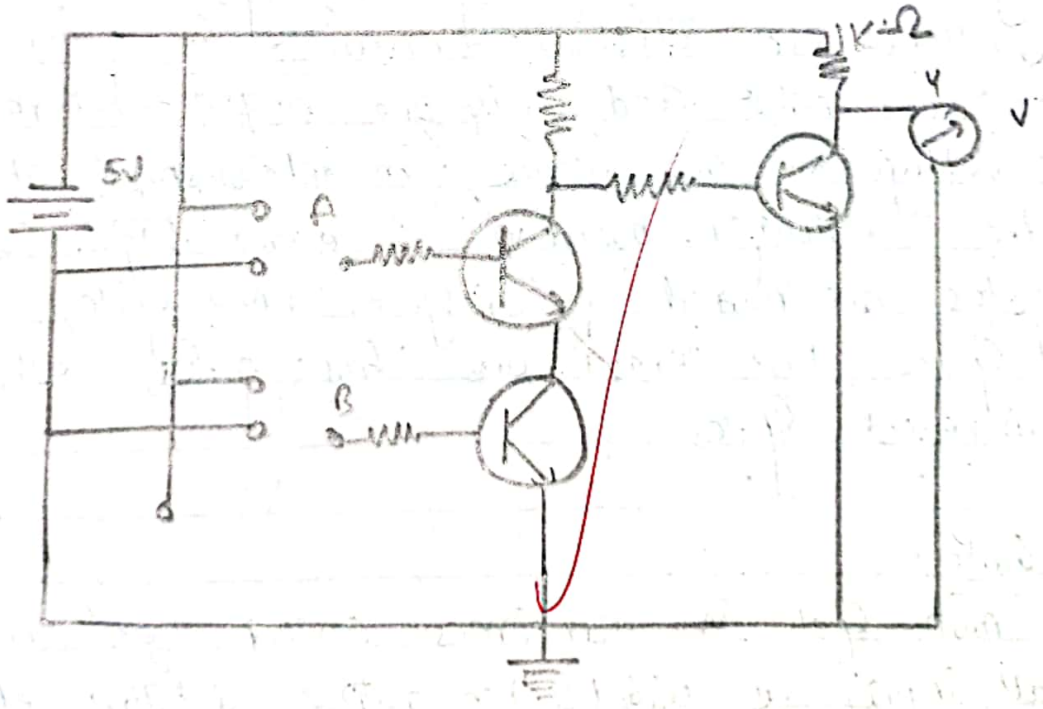


fig Experimental circuit diagram for AND gate

Boolean expression	Logical symbol	Truth Table		
		Inputs		Output
		A	B	Y
$Y = A.B$		0	0	0
		0	1	0
		1	0	0
		1	1	1

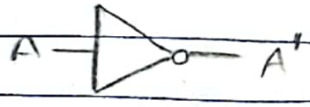
ii) OR Gate:

The OR Gate is sometimes called 'any or all' gate. When all inputs are low, then output is low else output is HIGH.

Boolean expression	Logic symbol	Truth Table		
		Inputs		Output
		A	B	Y
$Y = A+B$		0	0	0
		0	1	1
		1	0	1
		1	1	1

iii) NOT Gate:

The NOT Gate is often called an Inverter. The NOT gate has only one input. It gives output as a complement of input.

Boolean expression	Logic diagram	Truth Table	
		Input	Output
		A	Y
$Y = \bar{A}$		0	1
		1	0

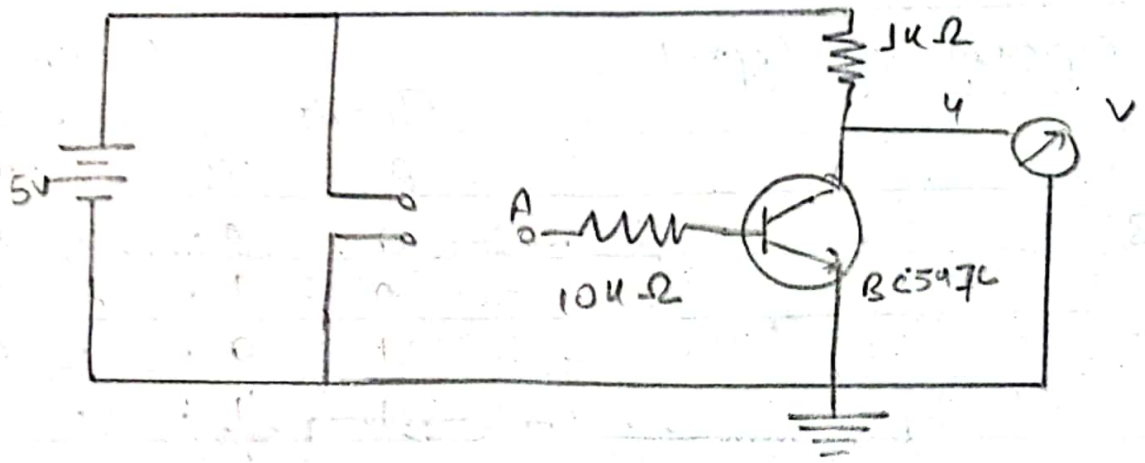


fig. Experimental circuit diagram for NOT gate

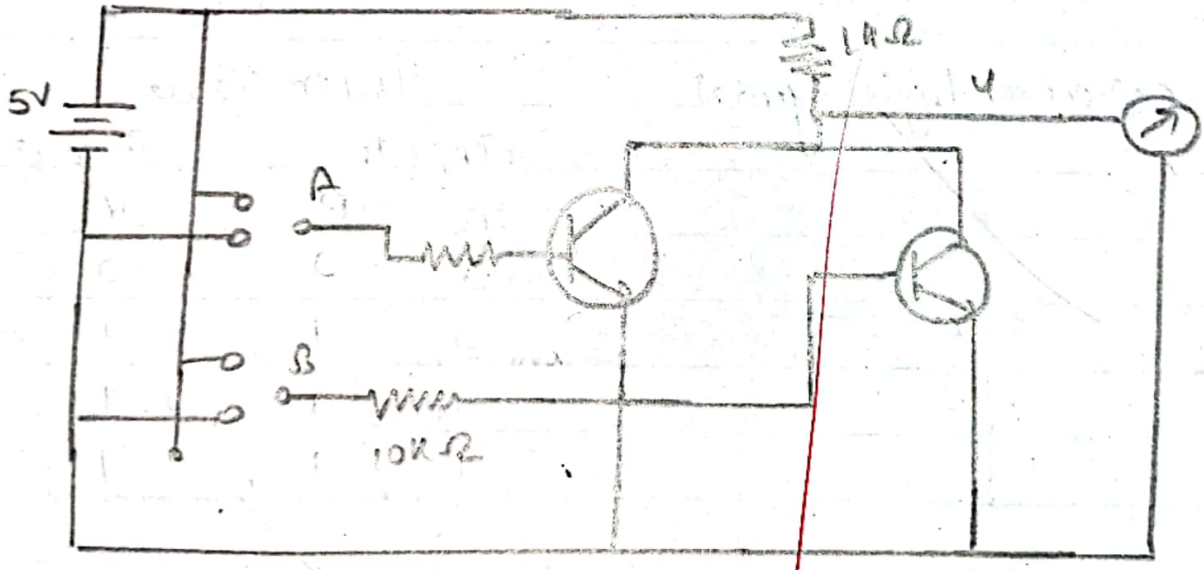
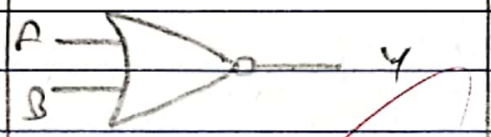


fig. Experimental circuit diagram for NOR gate

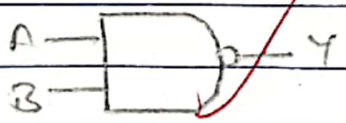
iv) NOR Gate:

It is the combination of OR & NOT gate which produces 'high' output if all input are 'low' otherwise 'low' output.

Boolean expression	Logic diagram	Truth Table		
		Inputs		Output
		A	B	Y
		0	0	1
$Y = (\overline{A+B})$		0	1	0
		1	0	0
		1	1	0

v) NAND Gate:

It is the combination of AND gate and NOT gate which produces low output if all input are 'HIGH'. It produces high output if any one of the input is 'low'.

Boolean expression	Logic diagram	Truth Table		
		Inputs		Output
		A	B	Y
		0	0	1
$Y = (\overline{AB})$		0	1	1
		1	0	1
		1	1	0

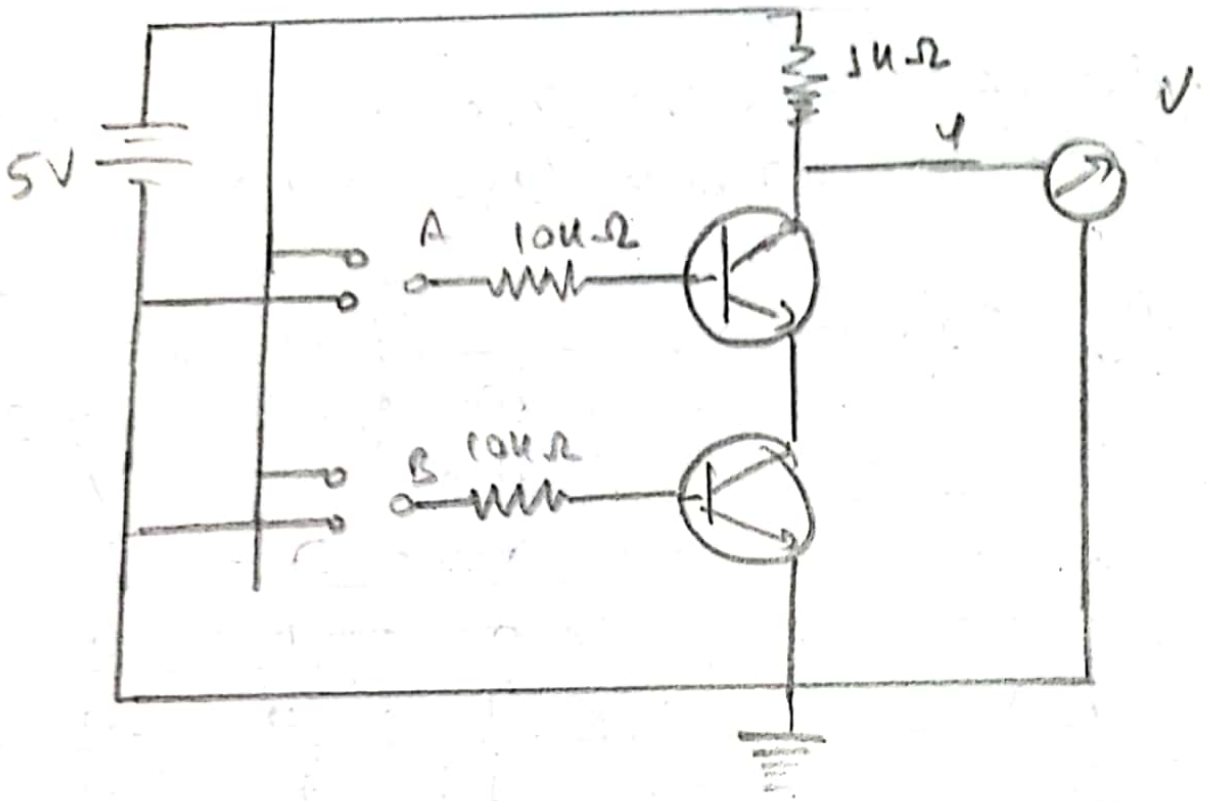


fig. Experimental circuit diagram for NAND gate

OBSERVATIONS:

Least count of voltmeter = 0.1 V
Least count of ammeter = 0.1 A

Table 1: OR Gate

SN	Inputs		Output
	A (volt)	B (volt)	Y (volt)
1	0	0	0
2	0	3.2	3
3	3.2	0	3
4	3.2	3.2	3

Table 2: AND Gate:

SN	Inputs		Output
	A (volt)	B (volt)	Y (volt)
1	0	0	0
2	0	3.2	0.2
3	3.2	0	0.2
4	3.2	3.2	3

Table 3: NOT Gate:

SN	Input	Output
	A (volt)	B (volt)
1	0	3.4
2	3.4	0

Table 4: NOR Gate.

SN	Inputs		Output
	A (volt)	B (volt)	Y (volt)
1	0	0	3
2	0	3.3	0.5
3	3.2	0	0.5
4	3.2	3.2	0.5

Table 5: NAND Gates

SN	Inputs		Output
	A (volt)	B (volt)	Y (volt)
1	0	0	3
2	0	3.3	3.1
3	3.3	0	3.1
4	3.3	3.3	0.1

RESULT:

↳ FOR NOT Gate:
When the input is 0, the output is 3.4 and vice versa.

↳ FOR OR Gate:
When both inputs are 0, the output is also 0 and when both or any one of the input is 3.2V, the output is 3V.

For AND gate:
When both inputs are 3.3, the output is 3 and when both or any of the inputs is 0, the output is 0 & 0.2V

For NAND gate:
When both the inputs are 0, output is 3V
When both inputs are 3.3V, output is 0.1V &
when either of the inputs are 0, output is 3.1 V.

For NOR gate:
When both inputs are 0, output is 3 & when both inputs or either one input is 3.2V, the output is 0.5V.

CONCLUSION:
Hence, the logic gates OR, AND, NOR, NOT & NAND can be studied & designed using TTL.

PRECAUTIONS:

i) The wire should not be loose in the breadboard.
ii) The voltage supply must be checked before hand.
iii) Transistors need to be connected properly.